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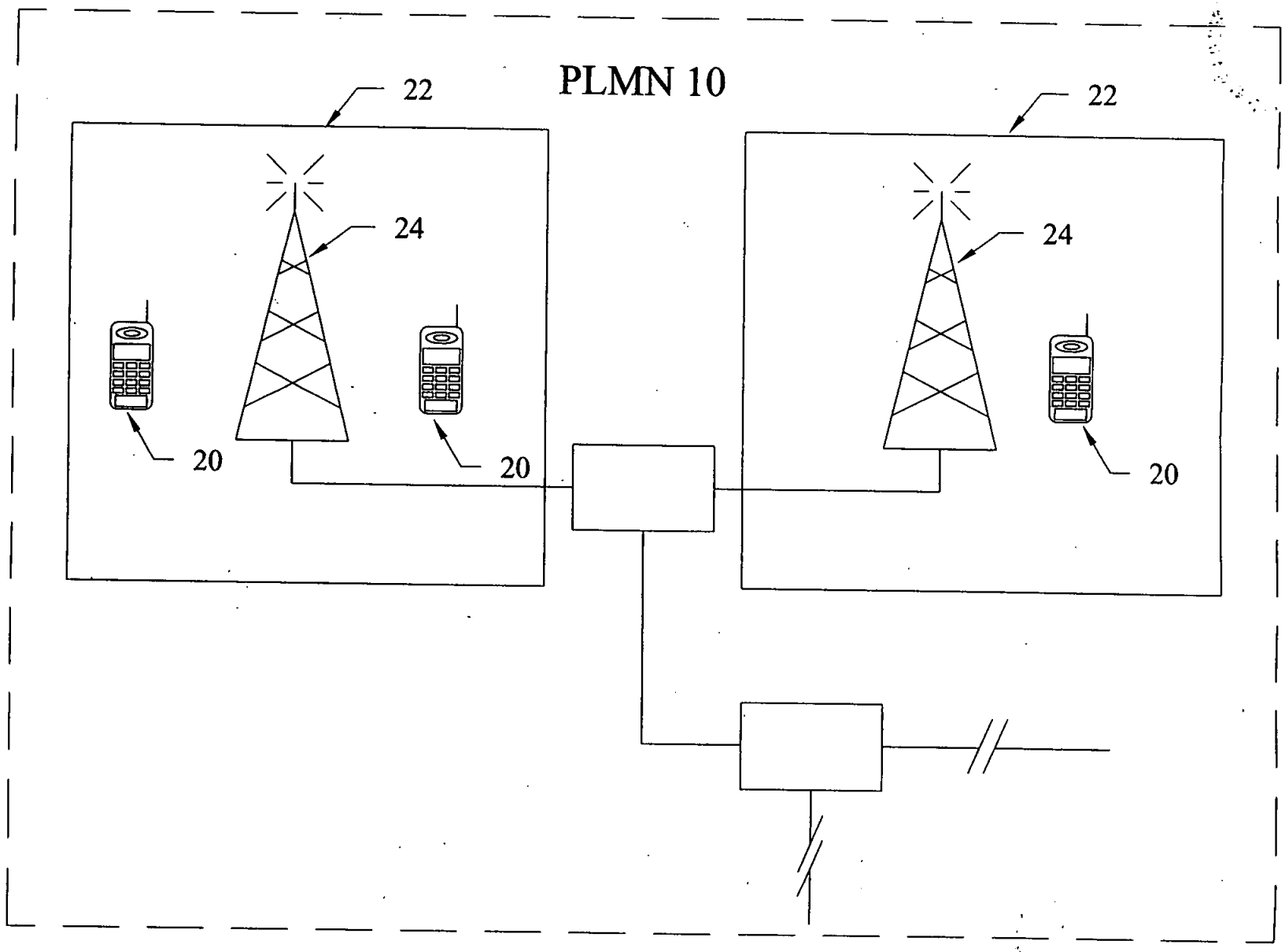



FIG. 1

Fig. 2

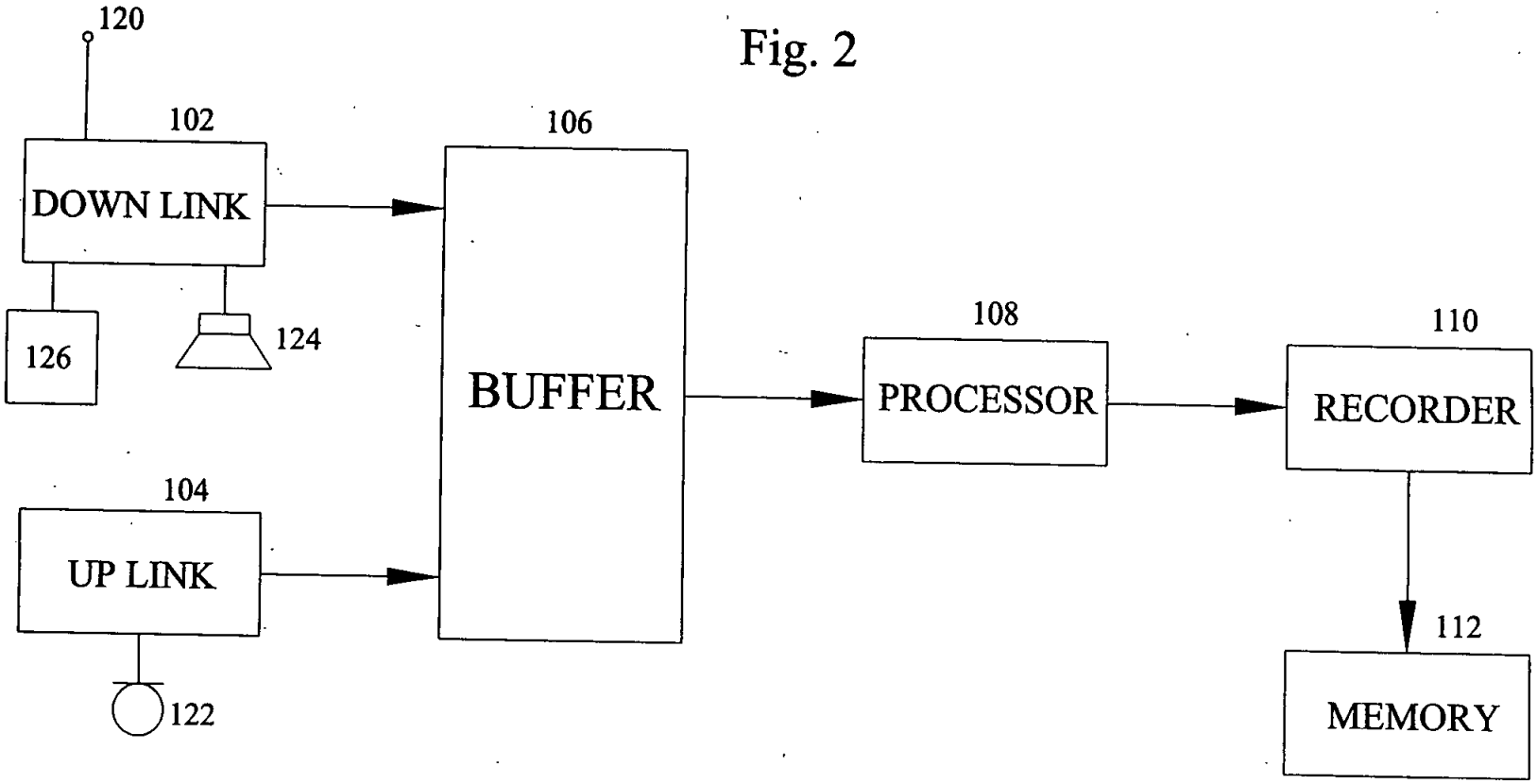

120
102
DOWN LINK
126
124
104
UP LINK
122
106
BUFFER
108
PROCESSOR
110
RECORDER
112
MEMORY

Fig. 3

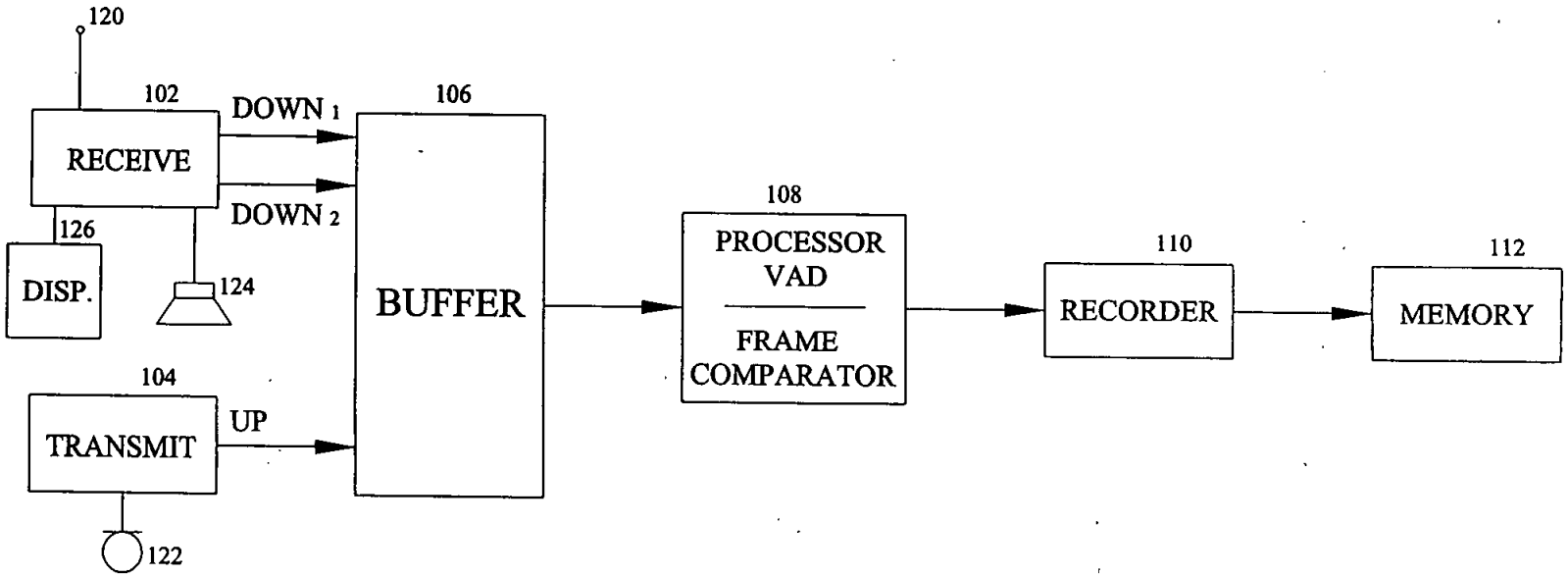
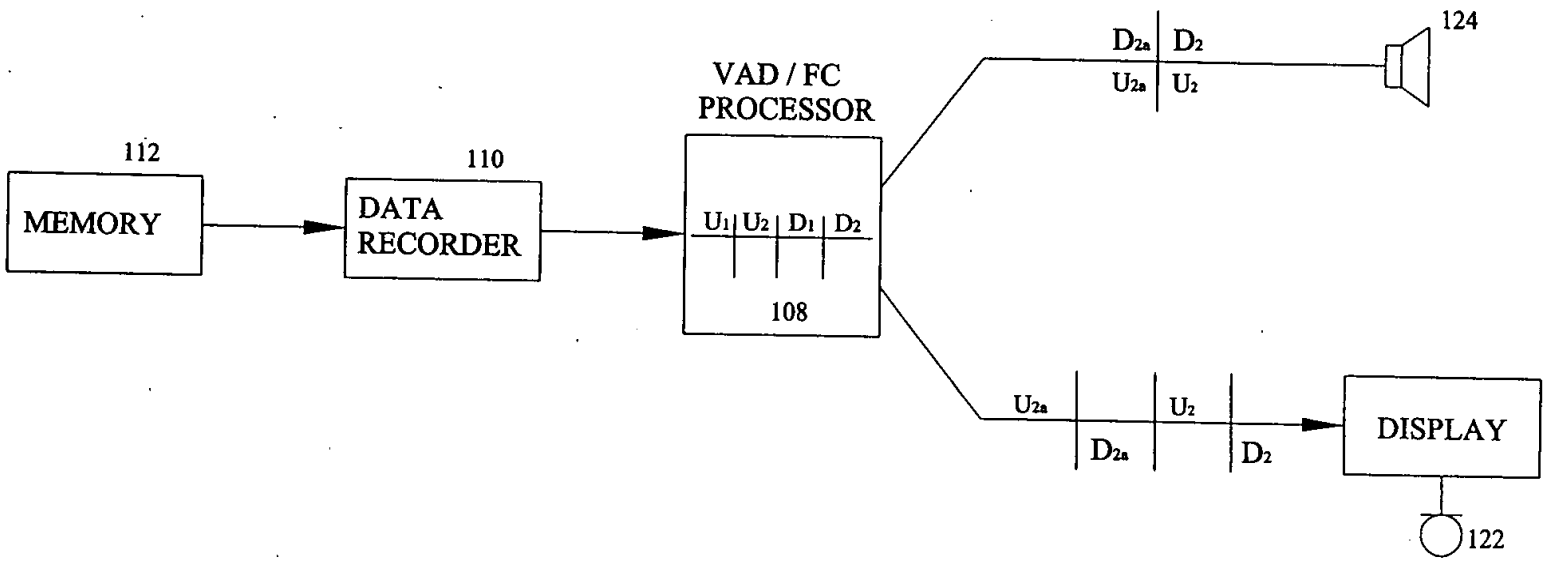

120
102
RECEIVE
DOWN 1
DOWN 2
106
BUFFER
126
DISP.
124
104
TRANSMIT
UP
122
108
PROCESSOR
VAD
FRAME
COMPARATOR
110
RECORDER
112
MEMORY

Fig 4


112
MEMORY
110
DATA RECORDER
VAD / FC PROCESSOR
U1 U2 D1 D2
108
D2a D2
U2a U2
124
U2a U2
D2a D2
DISPLAY
122